

## N-Channel 25 V (D-S) MOSFET

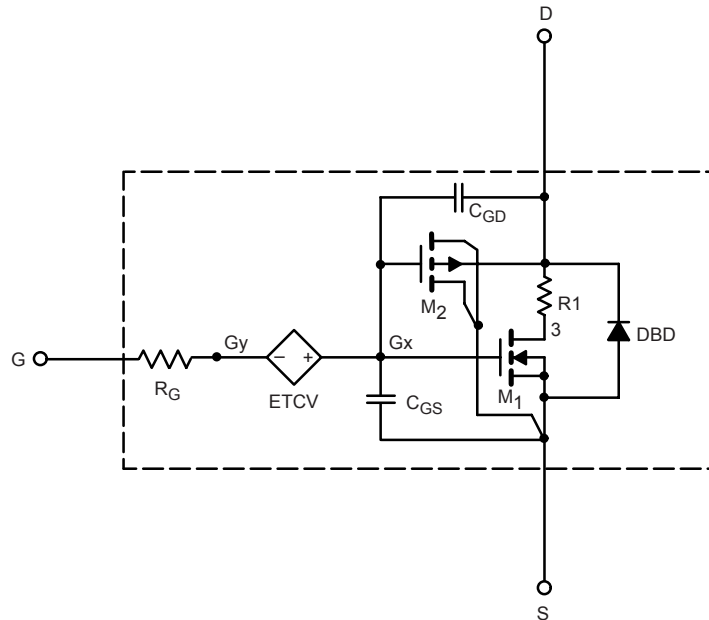
### DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

### SUBCIRCUIT MODEL SCHEMATIC



### Note

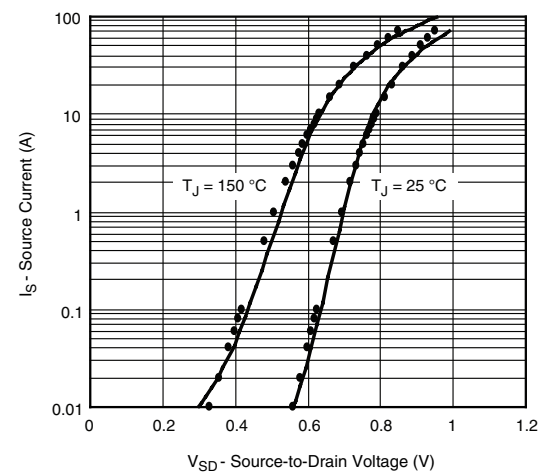
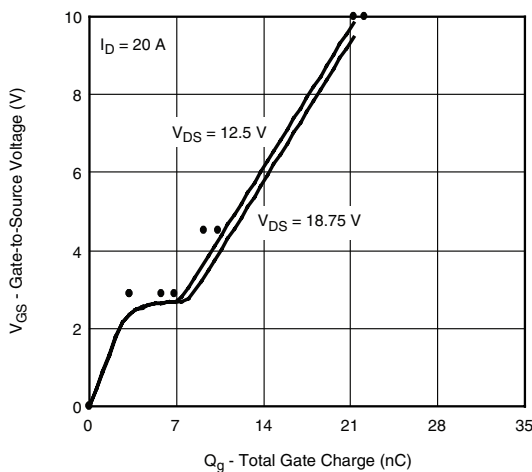
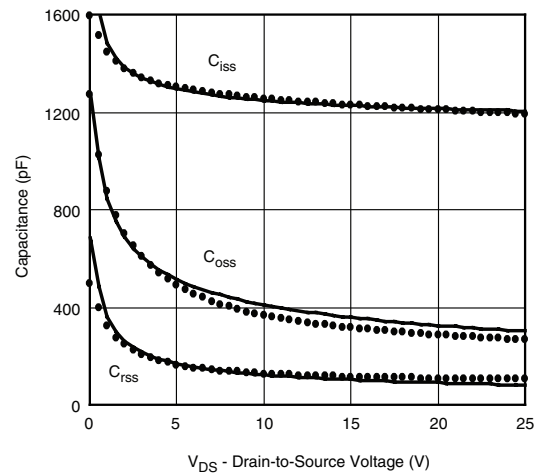
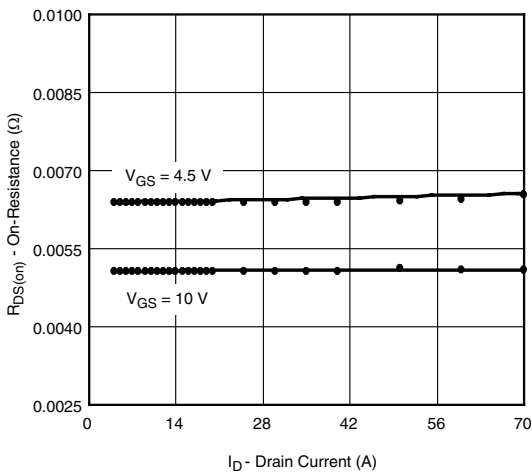
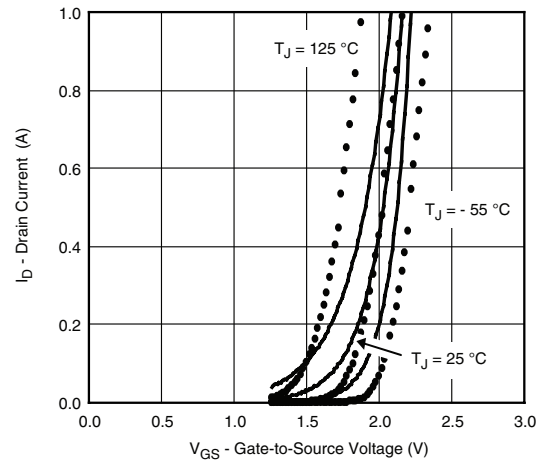
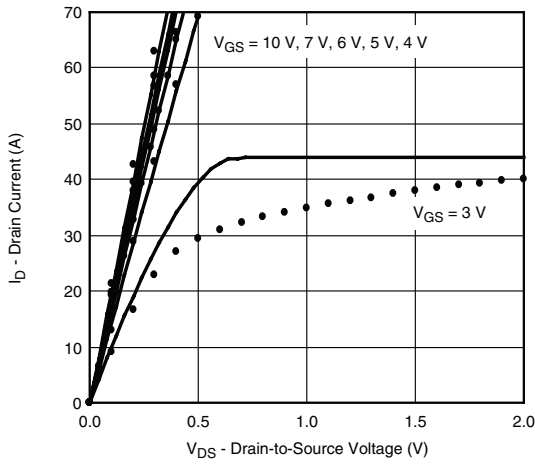
This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

| <b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted |              |  |                |               |          |
|---|--------------|--|----------------|---------------|----------|
| PARAMETER   | SYMBOL       | TEST CONDITIONS  | SIMULATED DATA | MEASURED DATA | UNIT     |
| <b>Static</b>   |              |  |                |               |          |
| Gate-Source Threshold Voltage   | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$                    | 1.2            | -             | V        |
| Drain-Source On-State Resistance <sup>a</sup>                                   | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 20\text{ A}$                          | 0.0051         | 0.0052        | $\Omega$ |
|   |              | $V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$                         | 0.0064         | 0.0064        |          |
| Forward Transconductance <sup>a</sup>   | $g_{fs}$     | $V_{DS} = 15\text{ V}, I_D = 20\text{ A}$                          | 74             | 85            | S        |
| Diode Forward Voltage <sup>a</sup>  | $V_{SD}$     | $I_S = 4\text{ A}$   | 0.74           | 0.75          | V        |
| <b>Dynamic<sup>b</sup></b>  |              |  |                |               |          |
| Input Capacitance   | $C_{iss}$    | $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$      | 1230           | 1230          | pF       |
| Output Capacitance  | $C_{oss}$    |  | 358            | 315           |          |
| Reverse Transfer Capacitance  | $C_{rss}$    |  | 102            | 115           |          |
| Total Gate Charge   | $Q_g$        | $V_{DS} = 12.5\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$  | 21             | 21.5          | nC       |
| Gate-Source Charge  | $Q_{gs}$     | $V_{DS} = 12.5\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$ | 10             | 9.3           |          |
| Gate-Source Charge  | $Q_{gs}$     |  | 3.2            | 3.2           |          |
| Gate-Drain Charge   | $Q_{gd}$     |  | 2.6            | 2.6           |          |

**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

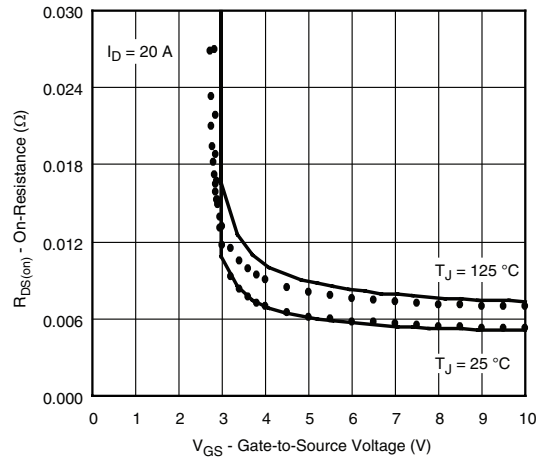
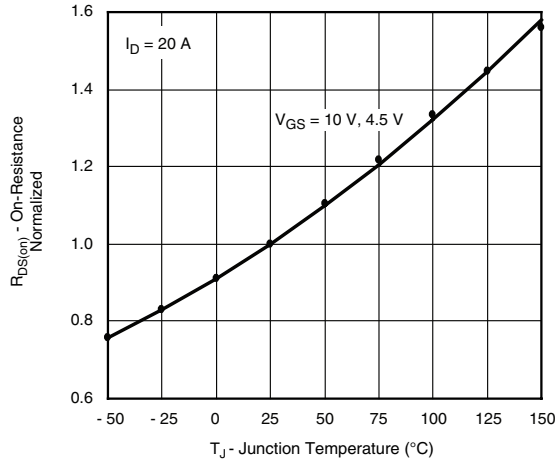
## COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted



### Note

Dots and squares represent measured data.

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## Disclaimer

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